Patent claims

1. A semiconductor component with trench isolation for defining active regions in a semiconductor substrate (1, 2, 3),
the trench isolation (STI, TTI) having a deep isolation trench with a covering insulation layer (10, 11) a side wall insulation layer (6) and an electrically conductive filling layer, which is electrically connected to a predetermined doping region of the semiconductor substrate in a bottom region of the isolation trench,
characterized by
a trench contact (DTC), which has a deep contact trench with a side wall insulation layer (6) and an electrically conductive filling layer (7), which is likewise electrically connected to the predetermined doping region of the semiconductor substrate (1, 2, 3) in a bottom region of the contact trench.

2. The semiconductor component as claimed in patent claim 1,
wherein the covering insulation layer (10, 11) is formed essentially below a semiconductor substrate surface and within the isolation trench.

3. The semiconductor component as claimed in patent claim 1 or 2,
wherein the trench isolation (STI, TTI) and the trench contact (DTC) have a larger depth than an associated depletion zone in the semiconductor substrate (1, 2, 3).

4. The semiconductor component as claimed in one of patent claims 1 to 3,
wherein the trench isolation (STI) has a widened, shallow isolation trench at the semiconductor

substrate surface for the purpose of filling non-active regions.

5. The semiconductor component as claimed in one of patent claims 1 to 4, wherein the predetermined doping region constitutes a doping well (2) of a multiple well structure.

6. The semiconductor component as claimed in one of patent claims 1 to 5, wherein the semiconductor substrate (1, 2, 3) has Si, the covering and side wall insulation layer (6, 10, 11) has SiO_2 and the filling layer (7) has highly doped polysilicon.

7. A method for fabricating a semiconductor component with trench isolation having the following steps:

a) Preparation of a semiconductor substrate (1, 2, 3) with at least one predetermined doping region (2);

b) Formation of deep trenches (T) as far as the predetermined doping region (2) for the purpose of realizing at least one trench isolation (STI, TTI) and a trench contact (DTC);

c) Formation of a side wall insulation layer (6) at the side walls of the trenches (T);

d) Formation of an electrically conductive filling layer (7) in the trenches (T);

e) Removal of at least the electrically conductive filling layer (7) in the upper region of the trenches for the trench isolation (STI, TTI) for the purpose of forming shallow trenches (ST); and

f) Formation of a covering insulation layer (10, 11) in the shallow trenches (ST) of the trench isolation (STI, TTI).

8. The method as claimed in patent claim 7,

wherein, in step a), a double or triple well structure is formed in the semiconductor substrate.

9. The method as claimed in patent claim 7 or 8, wherein, in step b), the deep trenches (T) are formed using a first hard mask layer (5) by means of an anisotropic etching method in the semiconductor substrate.

10. The method as claimed in one of patent claims 7 to 9, wherein, in step c), a thermal oxidation is carried out in order to form a trench insulation layer and an anisotropic etching method is carried out in order to remove a bottom region of the trench insulation layer.

11. The method as claimed in one of patent claims 7 to 10, wherein, in step d), a highly doped semiconductor material (7) having the same conduction type (n) as the predetermined doping region (2) is deposited.

12. The method as claimed in one of patent claims 7 to 11, wherein, in step e), in order to realize a widened trench isolation (STI), the conductive filling layer (7), the side wall insulation layer (6) and adjoining regions of the semiconductor substrate (1, 2, 3) are removed in the upper region of the deep trenches (T).

13. The method as claimed in one of patent claims 7 to 12, wherein, in step e), in order to realize a narrow trench isolation (TTI), only the conductive filling layer (7) with or without the side wall

insulation layer (6) is removed in the upper region of the trenches.

14. The method as claimed in one of patent claims 7 to 12,
wherein, in step f), an oxidation is carried out in order to form a first covering insulation partial layer (10) and/or a deposition is carried out in order to form a second covering insulation partial layer (11) in the shallow trench (ST).